

## EXPRESS MAIL LABEL NO. EV674901312US

PATENTS

# Attorney Docket No.: ELM-2 DIV. 6

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Glenn J. Leedy

Application No.: 10/614,067 Confirmation No.: 8117

Filed : July 3, 2003

For : THREE DIMENSIONAL STRUCTURE INTEGRATED

CIRCUIT

Group Art Unit : 2822

Examiner : Pamela E. Perkins

Mail Stop RCE

Commissioner for Patents

US 5,119,164

P.O. Box 1450

Alexandria, Virginia 22313-1450

## INFORMATION DISCLOSURE STATEMENT

### Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicant wishes to call the attention of the Examiner to the following documents:

U.S. Patent Documents

US	3,636,358	01/18/1972	Groschwitz	(6)
US	3,932,932	01/20/1976	Goodman	(2)
US	4,028,547	06/07/1977	Eisenberger	(3)
US	4,393,127	07/12/1983	Greschner et al.	(3)
US	4,528,072	07/09/1985	Kurosawa et al.	(2)
US	4,566,037	01/21/1986	Takatsu et al.	(6)
US	4,604,162	08/05/1986	Sobczak	
US	4,622,632	11/11/1986	Tanimoto et al.	(6)
US	4,810,889	03/07/1989	Yokomatsu et al.	(3)
US	4,849,857	07/18/1989	Butt et al.	
US	4,928,058	05/22/1990	Williamson	
US	4,990,462	02/05/1991	Sliwa	
US	5,051,326	09/24/1991	Celler et al.	(3)
US	5,110,712	05/05/1992	Kessler et al.	

06/02/1992 Sliwa et al.

# U.S. Patent Documents

US	5,166,962	11/24/1992	Murooka et al.	(3)
US	5,169,805	12/08/1992	Mok et al.	(4)
US	5,188,706	02/23/1993	Hori et al.	(3)
US	5,245,277	09/14/1993	Furtek et al.	(6)
US	5,283,107	02/01/1994	Bayer et al.	(6)
US	5,284,804	02/08/1994	Moslehi	
US	5,293,457	03/08/1994	Arima et al.	(6)
US	5,399,505	03/21/1995	Dasse et al.	(6)
US	5,432,999	07/18/1995	Capps et al.	(5)
US	5,450,603	09/12/1995	Davies	(6)
US	5,470,693	11/28/1995	Sachdev et al.	
US	5,517,457	05/14/1996	Sakui et al.	
US	5,572,689	11/05/1996	Gallup et al.	(6)
US	5,577,050	11/19/1996	Bair et al.	(1)
US	5,615,163	03/25/1997	Sakui et al.	
US	5,745,673	04/28/1998	Di Zenzo et al.	(1)
US	5,786,629	07/28/1998	Faris	
US	5,818,748	10/06/1998	Bertin et al.	(1)
US	6,092,174	07/18/2000	Roussakov	(6)
US	6,154,809	11/28/2000	Ikenaga et al.	(6)
US	6,301,653	10/09/2001	Mohamed et al.	(6)
US	· ·	10/09/2001	Sobel et al.	(6)
US	6,320,593	11/20/2001	Sobel et al.	(6)
US	2005-00223656	02/03/2005	Leedy	(6)
US	•	03/12/2002	Faris	
US	6,894,392	05/17/2005	Gudesen et al.	(6)

# Foreign Patent Documents

FD	0 201	380	12/17/1986	Fairchild
ĿЕ	0 201	300	12/1//1900	Semiconductor Corp.
EΡ	0 224	418	06/03/1987	Fujitsu Limited
EΡ	0 419	898	04/03/1991	Siemens
				Aktiengesellschaft
EΡ	0 455	455	11/06/1991	AT&T Corp.
EP	0 487	302	05/27/1992	Shin-Etsu Handotai
	0 107	302	03/2//1332	Company Ltd.
EP	0 503	816	09/16/1992	Shin-Etsu Handotai
ш	0 303	010	03/10/1332	Company Ltd.
EΡ	0 518	774	12/16/1992	France Telecom (FR)
E D	0 526	551	02/10/1993	The Commonwealth of
EF	0 320	551	02/10/1993	Australia
EP	0 554	063	08/04/1993	Canon Kabushiki
EP	0 334	003	00/04/1993	Kaisha
ΕP	0 555	252	08/18/1993	Fraunhofer Ges
r.	0 333	232	00/10/1993	Forschung (DE)
WO	89/01	0255	11/02/1989	3D Systems, Inc.

#### Foreign Patent Documents

WO 90/009093 08/23/1990 Polylithics, Inc. WO 92/017901 10/15/1992 Integrated System Assemblies Corp.

### Nonpatent Literature Documents

Jones, R.E., Jr. "An evaluation of methods for passivating silicon integrated circuits", April 1972; pp. 23-8

Svechnikov, S.V.; Kobylyatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzovlev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminum membrane crossings of conductors"; 1972

Sun, R.C.; Tisone, T.C.; Cruzan, P.D.; "Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)"; March 1973; pp. 1009-16

Wade, T.E.; "Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection"; 1982; pp. 516-19

Boyer, P.K.; Collins, G.J.; Moore, C.A.; Ritchie, W.K.; Roche, G. A.; Solanski, R. (A); Tang, C.C.; "Microelectronic thin film deposition by ultraviolet laser photolysis MONOGRAPH TITLE - Laser processing of semiconductor devices"; 1983; pp. 120-126

Boyer, P.K.; Moore, C.A.; Solanki, R.; Ritchie, W.K.; Roche, G.A.; Collins, G.J.; "Laser photolytic deposition of thin films"; 1983; pp. 119-27

Chen, Y.S.; Fatemi, H.; "Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits"; May-June 1986; pp. 645-9

Salazar, M.; Wilkins, C.W., Jr.; Ryan, V.W.; Wang, T.T.; "Low stress films of cyclized polybutadiene dielectrics by vacuum annealing"; Oct. 21-22, 1986; pp. 96-102

Townsend, P.H.; Huggins, R.A.; "Stresses in borophosphosilicate glass films during thermal cycling"; Oct. 21-22, 1986; pp. 134-41

## Nonpatent Literature Documents

Wolf, Stanley and Richard N. Tauber; Silicon Processing For the VLSI Era, Volume 1: Process Technology; Sunset Beach, CA: Lattice Press, 1986, pages 191-194 (6)

Pai, Pei-Lin; "Multilevel Interconnection Technologies--A Framework And Examples"; 1987; pp. 1871

Pei-lin Pai; Chetty, A.; Roat, R.; Cox, N.; Chiu Ting; "Material characteristics of spin-on glasses for interlayer dielectric applications"; November 1987, pp. 2829-34

Riley, P.E.; Shelley, A.; "Characterization of a spin-applied dielectric for use in multilevel metallization"; May 1988; pp. 1207-10

Tamura, H.; Nishikawa, T.; Wakino, K.; Sudo, T.; "Metalized MIC substrates using high K dielectric resonator materials"; October 1988; pp. 117-126

Allen, Mark G.,; Senturia, Stephen D.; "Measurement of polyimide interlayer adhesion using microfabricated structures"; 1988; pp. 352-356

Chang, E.Y.; Cibuzar, G.T.; Pande, K.P.; "Passivation of GaAs FET's with PECVD silicon nitride films of different stress states"; September 1988; pp. 1412-18

Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR); "Electrophysical investigation of thin-layered inorganic coatings"; 1989; pp. 826-828

Reche, J.J. H.; "Control of thin film materials properties used in high density multichip interconnect"; April 24-28, 1989; p. 494

Maw, T.; Hopla, R.E.; "Properties of a photoimageable thin polyimide film"; Nov. 26-29-, 1990; pp. 71-6

Guckel, H.; "Surface micromachined pressure transducers"; 1991; pp. 133-146

Draper, B. L.; Hill, T.A.; "Stress and stress relaxation in integrated circuit metals and dielectrics"; July-Aug. 1991; pp. 1956-62

#### Nonpatent Literature Documents

Garino, T.J.; Harrington, H. M.; "Residual stress in PZT thin films and its effect on ferroelectric properties'; 1992; pp. 341-7

The aforementioned references are listed on the accompanying Form PTO/SB/08 (submitted in duplicate). Pursuant to 37 C.F.R. 1.98 (a)(2), applicant is not submitting copies of the aforementioned U.S. patent document references. Copies of the aforementioned Foreign Patent Documents and Non-Patent Literature Documents are enclosed herewith.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

The aforementioned U.S. Patent Documents identified by (1) were cited in an Office Action mailed on October 18, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/143,200. Documents identified by (2) were cited in an Office Action mailed on November 17, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/742,057. Documents identified by (3) were cited in an Office Action mailed on December 7, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/766,557. The Document identified by (4) was cited in an Office Action mailed on December 13, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/742,282. The document identified by (5) was cited in an Office Action mailed on December 19, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/379,820. The U.S. Patent Documents and

Nonpatent Literature Documents identified by (6) were cited in an Office Action mailed on January 26, 2006 in co-pending commonly assigned U.S. Patent Application No. 10/741,647.

It is respectfully requested that these references be: (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO-SB/08, as considered and initialed by the Examiner, be returned with the next communication.

This Statement is submitted concurrently with a request for continued examination under 37 C.F.R. §1.114. Pursuant to 37 C.F.R. §1.97(b)(4), applicant believes no fee is due in connection with this statement. However, if for any reason a fee is due, the Director is hereby authorized to charge payment of any fees required in connection with this Statement, or to credit any overpayment of the same, to Deposit Account No. 06-1075 (Order No.: 001202-0132). A duplicate copy of this Statement is enclosed herewith.

 $\,$  An early and favorable action is respectfully requested.

Respectfully submitted,

Jeffrey D Mullen

Registration. No. 52,056

Agent for Applicant

Fish & Neave IP Group

Ropes & Gray LLP

Customer No. 1473

1251 Avenue of the Americas New York, New York 10020-1105

Tel.: (212) 596-9000

Fax: (212) 596-9090

Express Mail Label No. EV674901312US

stitute for form 1449A/B/PTO

PTO/SB/08a/b (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Examiner Name

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

10/614,067 (Conf. No. 8117) Application Number July 3, 2003 Filing Date First Named Inventor Leedy 2822 Art Unit Pamela Perkins

Complete if Known

(Use as many sheets as necessary)

ELM-2 Div. 6 3 Attorney Docket Number Sheet

			U.S. PA	TENT DOCUMENTS	
Examiner	Cite	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where Relevant Passages or Relevant
Initials*	No.1	Number-Kind Code <sup>2</sup> ( if known)	MM-DD-YYYY	Applicant of Cited Document	Figures Appear
		US 3,636,358	01/18/1972	Groschwitz	
		US 3,932,932	01/20/1976	Goodman	
		US 4,028,547	06/07/1977	Eisenberger	
		US 4,393,127	07/12/1983	Greschner et al.	
		US 4,528,072	07/09/1985	Kurosawa et al.	
		US 4,566,037	01/21/1986	Takatsu et al.	
		US 4,604,162	08/05/1986	Sobczak	
·		US 4,622,632	11/11/1986	Tanimoto et al.	
		US 4,810,889	03/07/1989	Yokomatsu et al.	
		US 4,849,857	07/18/1989	Butt et al.	
		US 4,928,058	05/22/1990	Williamson	
		US 4,990,462	02/05/1991	Sliwa	
		US 5,051,326	09/24/1991	Celler et al.	
	i	US 5,110,712	05/05/1992	Kessler et al.	
		US 5,119,164	06/02/1992	Sliwa et al.	
		US 5,166,962	11/24/1992	Murooka et al.	
		US 5,169,805	12/08/1992	Mok et al.	
		US 5,188,706	02/23/1993	Hori et al.	
		US 5,245,277		Furtek et al.	
		US 5,283,107	02/01/1994	Bayer et al.	
		US 5,284,804	02/08/1994	Moslehi	
		US 5,293,457	03/08/1994	Arima et al.	
		US 5,399,505	03/21/1995	Dasse et al.	
		US 5,432,999	07/18/1995	Capps et al.	
		US 5,450,603	09/12/1995	Davies	
		US 5,470,693	11/28/1995	Sachdev et al.	
		US 5,517,457	05/14/1996	Sakui et al.	
	·	US 5,572,689	11/05/1996	Gallup et al.	
		US 5,577,050	11/19/1996	Bair et al.	
		US 5,615,163	03/25/1997	Sakui et al.	
		US 5,745,673	04/28/1998	Di Zenzo et al.	
	<b></b>	US 5,786,629	07/28/1998	Faris	
		US 5,818,748	10/06/1998	Bertin et al.	
		US 6,092,174	07/18/2000	Roussakov	
	<u> </u>	US 6,154,809	11/28/2000	Ikenaga et al.	
		US 6,301,653	10/09/2001	Mohamed et al.	
		US 6,300,935	10/09/2001	Sobel et al.	
		US 6,320,593	11/20/2001	Sobel et al.	
		US 2005-00223656	02/03/2005	Leedy	-
	<del> </del>	US 6,355,976	03/12/2002	Faris	
		US 6,894,392	05/17/2005	Gudesen et al.	

Examiner	Date
Signature	Considered
0.0	

PTO/SB/08a/b (08-03)

Approved for use through 07/31/2006. OMB 0551-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Sub	stitute for form 1449A/B/PT	0		Complete if Known		
00.	Salato for form 1440702.	•		Application Number	10/614,067 (Conf. No. 8117)	
11	<b>IFORMATION</b>	I DI	SCLOSURE	Filing Date	July 3, 2003	
S	TATEMENT B	3Y /	APPLICANT	First Named Inventor	Leedy	
				Art Unit	2822	
	(Use as many she	eets as	necessary)	Examiner Name	Pamela Perkins	
Sheet	Sheet 2 of 3			Attorney Docket Number	ELM-2 Div. 6	

		FOREI	GN PATENT	DOCUMENTS		
Examiner	Cite	Foreign Patent Document	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where Relevant Passages	T6
Initials*	No.1	Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	MM-DD-YYYY	Applicant of Cited Document	or Relevant Figures Appear	
		EP 0 201 380	12/17/1986	Fairchild Semiconductor Corp.		
		EP 0 224 418	06/03/1987	Fujitsu Limited		
		EP 0 419 898	04/03/1991	Siemens Aktiengesellschaft		<u>L</u> .
		EP 0 455 455	11/06/1991	AT&T Corp.		L_
	1	EP 0 487 302	05/27/1992	Shin-Etsu Handotai Company Ltd.		
	1	EP 0 503 816	09/16/1992	Shin-Etsu Handotai Company Ltd.		
		EP 0 518 774	12/16/1992	France Telecom (FR)		
		EP 0 526 551	02/10/1993	The Commonwealth of Australia		
		EP 0 554 063	08/04/1993	Canon Kabushiki Kaisha		1
		EP 0 555 252	08/18/1993	Fraunhofer Ges Forschung (DE)		<u> </u>
		WO 89/ 10255	11/02/1989	3D Systems, Inc.		
		WO 90/ 09093	08/23/1990	Polylithics, Inc.		
		WO 92/ 17901	10/15/1992	Integrated System Assemblies Corp.		

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		Jones, R.E., Jr. "An evaluation of methods for passivating silicon integrated circuits", April 1972; pp. 23-8	
		Svechnikov, S.V.; Kobylyatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzovlev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminum membrane crossings of conductors"; 1972	
		Sun, R.C.; Tisone, T.C.; Cruzan, P.D.; "Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)"; March 1973; pp. 1009-16	
		Wade, T.E.; "Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection"; 1982; pp. 516-19	
		Boyer, P.K.; Collins, G.J.; Moore, C.A.; Ritchie, W.K.; Roche, G. A.; Solanski, R. (A); Tang, C.C.; "Microelectronic thin film deposition by ultraviolet laser photolysis MONOGRAPH TITLE - Laser processing of semiconductor devices"; 1983; pp. 120-126	
		Boyer, P.K.; Moore, C.A.; Solanki, R.; Ritchie, W.K.; Roche, G.A.; Collins, G.J.; "Laser photolytic deposition of thin films"; 1983; pp. 119-27	
		Chen, Y.S.; Fatemi, H.; "Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits"; May-June 1986; pp. 645-9	
		Salazar, M.; Wilkins, C.W., Jr.; Ryan, V.W.; Wang, T.T.; "Low stress films of cyclized polybutadiene dielectrics by vacuum annealing"; Oct. 21-22, 1986; pp. 96-102	
		Townsend, P.H.; Huggins, R.A.; "Stresses in borophosphosilicate glass films during thermal cycling"; Oct. 21-22, 1986; pp. 134-41	
		Wolf, Stanley and Richard N. Tauber; Silicon Processing For the VLSI Era, Volume 1: Process Technology; Sunset Beach, CA: Lattice Press, 1986, pages 191-194	

Examiner	Date	
Signature	Considered	

# Express Mail Label No. EV674901312US

PTO/SB/08a/b (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Sub	estitute for form 1449A/B/P	το		Complete if Known		
000	Salato for form 1440/02/	. •		Application Number	10/614,067 (Conf. No. 8117)	
l in	NFORMATIO	N DI	SCLOSURE	Filing Date	July 3, 2003	
S	TATEMENT	BY A	APPLICANT	First Named Inventor	Leedy	
				Art Unit	2822	
	(Use as many sheets as necessary)			Examiner Name	Pamela Perkins	
Sheet	3	of	3	Attorney Docket Number ELM-2 Div. 6		

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		Pai, Pei-Lin; "Multilevel Interconnection TechnologiesA Framework And Examples"; 1987; pp. 1871	
		Pei-lin Pai; Chetty, A.; Roat, R.; Cox, N.; Chiu Ting; "Material characteristics of spin-on glasses for interlayer dielectric applications"; November 1987, pp. 2829-34	
		Riley, P.E.; Shelley, A.; "Characterization of a spin-applied dielectric for use in multilevel metallization"; May 1988; pp. 1207-10	
		Tamura, H.; Nishikawa, T.; Wakino, K.; Sudo, T.; "Metalized MIC substrates using high K dielectric resonator materials"; October 1988; pp. 117-126	
		Allen, Mark G.,; Senturia, Stephen D.; "Measurement of polyimide interlayer adhesion using microfabricated structures"; 1988; pp. 352-356	
		Chang, E.Y.; Cibuzar, G.T.; Pande, K.P.; "Passivation of GaAs FET's with PECVD silicon nitride films of different stress states"; September 1988; pp. 1412-18	
		Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR); "Electrophysical investigation of thin-layered inorganic coatings"; 1989; pp. 826-828	
		Reche, J.J. H.; "Control of thin film materials properties used in high density multichip interconnect"; April 24-28, 1989; p. 494	
		Maw, T.; Hopla, R.E.; "Properties of a photoimageable thin polyimide film"; Nov. 26-29-, 1990; pp. 71-6	
		Guckel, H.; "Surface micromachined pressure transducers"; 1991; pp. 133-146	
		Draper, B. L.; Hill, T.A.; "Stress and stress relaxation in integrated circuit metals and dielectrics"; July-Aug. 1991; pp. 1956-62	
		Garino, T.J.; Harrington, H. M.; "Residual stress in PZT thin films and its effect on ferroelectric properties'; 1992; pp. 341-7	

<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at <a href="https://www.uspto.gov">www.uspto.gov</a> or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

Examiner	Date
Signature	Considered
<b>\$14116.16.1</b>	